AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

Please cancel claim 14 without prejudice.

1. (CURRENTLY AMENDED) An apparatus comprising:

a first plurality of parallel switches configured to (i) each receive a multiphased data signal having N phases, where N is a positive integer and (ii) control a voltage on a first output pin; and

a second plurality of parallel switches configured to (i) each receive a digital complement of said multiphased data signal and (ii) control a voltage on a second output pin, wherein said first and second pluralities of parallel switches are configured to provide rise time control of a differential waveform.

2. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein a timing between a first and a last phase of said multiphased data signal is configured to determine a rise and fall time of said differential waveform.

3. (ORIGINAL) The apparatus according to claim 1, wherein each of said first and second pluralities of parallel switches are weighted to determine a pulse shape of said differential waveform.

4. (ORIGINAL) The apparatus according to claim 1, further comprising:

one or more current sources configured to provide current to each of said first and second pluralities of parallel switches.

5. (ORIGINAL) The apparatus according to claim 4, wherein said one or more current sources comprises parallel current sources.

6. (ORIGINAL) The apparatus according to claim 5, wherein each of said parallel current sources are weighted to determine a pulse shape of said differential waveform.

7. (ORIGINAL) The apparatus according to claim 1, further comprising:

a first driver configured in parallel; and

a second driver configured in parallel, wherein said first and second drivers are configured to synchronize to a phased clock signal.

8. (ORIGINAL) The apparatus according to claim 7, wherein said first and second drivers are configured to perform pre-emphasis on said differential waveform.

9. (CURRENTLY AMENDED) The apparatus according to claim 8, wherein said first and second drivers are configured to mitigate effects of ~~ISI~~ intersymbol interference (ISI).

10. (ORIGINAL) The apparatus according to claim 7, wherein said first driver comprises a main driver and said second driver comprises a secondary driver.

11. (ORIGINAL) The apparatus according to claim 7, wherein said first driver comprises one or more flip-flops and said second driver comprises one or more flip-flops.

12. (ORIGINAL) The apparatus according to claim 7, wherein said first and second drivers are clocked by a multiphase clock signal.

13. (ORIGINAL) The apparatus according to claim 12, further comprising:

a clock generation circuit configured to generate said multiphase clock in response to a data signal and a precompensation signal.

14. (CANCELED)

15. (CURRENTLY AMENDED) The apparatus according to claim ~~13~~ 1, wherein a first phase and a second phase of ~~said~~ a multiphase

clock signal are configured to set a rise and fall time for said differential waveform.

16. (PREVIOUSLY PRESENTED) The apparatus according to claim 15, wherein generation of said first phase and said second phase are controlled by a bias.

17. (ORIGINAL) The apparatus according to claim 1, wherein said apparatus is configured to overcome cable induced effects.

18. (ORIGINAL) The apparatus according to claim 1, wherein said apparatus is further configured to synchronize a plurality of drivers to provide precompensation.

19. (CURRENTLY AMENDED) An apparatus comprising:

means for controlling a voltage on a first output pin with a first plurality of parallel switches each receiving a multiphased data signal <u>having N phases, where N is a positive integer</u>;

means for controlling a voltage on a second output pin with a second plurality of parallel switches each receiving a digital complement of said multiphased data signal; and

means for providing rise time control of a differential waveform, wherein said first and second pluralities of parallel switches are driven by a phased data signal.

20. (CURRENTLY AMENDED) A method for implementing ~~SCSI~~ small computer systems interface (SCSI) equalization, comprising the steps of:

(A) controlling a voltage on a first output pin with a first plurality of parallel switches each receiving a multiphased data signal having N phases, where N is a positive integer;

(B) controlling a voltage on a second output pin with a second plurality of parallel switches each receiving a digital complement of said multiphased data signal; and

(C) providing rise time control of a differential waveform, wherein said first and second pluralities of parallel switches are driven by a phased data signal.

21. (PREVIOUSLY PRESENTED) An apparatus comprising:

a first plurality of parallel switches configured to control a voltage on a first output pin;

a second plurality of parallel switches configured to control a voltage on a second output pin, wherein said first and second pluralities of parallel switches are configured to provide rise time control of a differential waveform and are driven by a phased data signal;

a first driver and a second driver configured in parallel, wherein said first and second drivers (i) are configured to synchronize to a phased clock signal and (ii) are clocked by a multiphase clock signal; and

a clock generation circuit configured to generate said multiphase clock in response to a data signal and a precompensation signal, wherein a first phase and a second phase of said multiphase clock signal are configured to set a rise and fall time for said differential waveform.

22. (NEW) The apparatus according to claim 1, wherein said positive integer N, is three or more.